Patent Claims

1. A circuit for generating an asynchronous signal pulse having a predetermined duration at an output of an integrated circuit,
which has
a first and a second transistor (2, 3) in the integrated circuit, which are connected in series between a supply potential (U_{DD}) and ground (GND), firstly a control pulse (A) having the predetermined duration being present at a control connection (G1) of the first transistor (2) and then a control pulse (B) being present at a control connection (G2) of the second transistor (3), with the result that, for the predetermined duration, firstly the first transistor (2) and then the second transistor (3) is turned on and the connecting point (4) is firstly at the supply potential (U_{DD}) and then at ground (GND), and
a resistor (6, 7) for the definition of the active signal state, which is connected outside the integrated circuit in parallel with one of the two transistors (2, 3) in the integrated circuit either between the supply potential (U_{DD}) and the connecting point (4) or between ground (GND) and the connecting point (4).

2. The circuit as claimed in claim 1,
wherein
a waiting time (Δt) is provided between the first control pulse (A) and the second control pulse (B), in which the two pulses do not overlap.

3. The circuit as claimed in claim 1 or 2,
wherein
one of the two control pulses (B) is generated from the other of the two control pulses (A) by an inverter delay device.

4. The circuit as claimed in one of the preceding claims, wherein the first transistor (2) is a P-channel MOS transistor and the second transistor (3) is an N-channel MOS transistor, the control connection (G1) of the first transistor being inverted.

5. The circuit as claimed in claim 4, wherein the first transistor (2) and the second transistor (3) form a CMOS inverter with independent control gate connections.